## CLAIMS

We claim:

1. A semiconductor package comprising:

a substrate having a surface, said surface having a central region and an outer region;

a first plurality of electrical connections on said outer region spaced apart by a first distance; and,

a second plurality of electrical connections on said central region spaced apart by a second distance, wherein said second distance is smaller than said first distance.

2. The package of claim 1 wherein said first and second plurality of electrical connections are selected from the group comprising: input/output connections, power connections, and ground connections.

3. The package of claim 1 wherein said first and second plurality of electrical connections comprise an array of electrically conductive bumps.

4. The package of claim 1 wherein said first and second plurality of electrical connections comprise conductive lands.

5. The package of claim 1 further comprising a plurality of routing channels extending from said first and second plurality of electrical connections, wherein said

second electrical connections have more routing channels extending therefrom than said first electrical connections.

6. The package of claim 5 wherein said first plurality of electrical connections are spaced apart to allow at least four routing channels to pass between said first plurality of electrical connections, and said second plurality of electrical connections do not have a routing channel between said second plurality of electrical connections.

7. The package of claim 1 wherein said first and second electrical connections are positioned on said surface in a progressive pitch layout.

8. An integrated circuit comprising:

an integrated circuit die having a surface, said surface having a central region and an outer region;

a first plurality of leads on said outer region spaced apart by a first distance; and,

a second plurality of leads on said central region spaced apart by a second distance, wherein said second distance is smaller than said first distance.

9. The integrated circuit of claim 8 wherein said first and second plurality of electrical connections are selected from the group comprising: input/output connections, power connections, and ground connections.

10. The integrated circuit of claim 8 wherein said first and second plurality of electrical connections comprise an array of electrically conductive bumps.

11. The integrated circuit of claim 8 wherein said first and second plurality of electrical connections comprise conductive lands.

12. The integrated circuit of claim 8 further comprising a plurality of routing channels extending from said first and second plurality of electrical connections, wherein said second electrical connections have more routing channels extending therefrom than said first electrical connections.

13. The integrated circuit of claim 12 wherein said first plurality of electrical connections are spaced apart to allow at least four routing channels to pass between said first plurality of electrical connections, and said second plurality of electrical connections do not have a routing channel between said second plurality of electrical connections.

14. The integrated circuit of claim 8 wherein said first and second electrical connections are positioned on said surface in a progressive pitch layout.

15. A printed circuit board comprising:

a substrate having a surface, said surface having a central region and an outer region;

a first plurality of electrical connections on said outer region spaced apart by a first distance; and,

a second plurality of electrical connections on said central region spaced apart by a second distance, wherein said second distance is smaller than said first distance.

16. The printed circuit board of claim 15 wherein said first and second plurality of electrical connections are selected from the group comprising: input/output connections, power connections, and ground connections.

17. The printed circuit board of claim 15 wherein said first and second plurality of electrical connections comprise an array of electrically conductive bumps.

18. The printed circuit board of claim 15 wherein said first and second plurality of electrical connections comprise conductive lands.

19. The printed circuit board of claim 15 wherein said first and second plurality of electrical connections comprise connector pins.

20. The printed circuit board of claim 15 further comprising a plurality of routing channels extending from said first and second plurality of electrical connections, wherein said second electrical connections have more routing channels extending therefrom than said first electrical connections.

21. The printed circuit board of claim 20 wherein said first plurality of electrical connections are spaced apart to allow at least four routing channels to pass between said first plurality of electrical connections, and said second plurality of electrical

connections do not have a routing channel between said second plurality of electrical connections.

22. The printed circuit board of claim 15 wherein said first and second electrical connections are positioned on said surface in a progressive pitch layout.

23. An apparatus comprising:

a substrate having a surface, said surface having a central region and an outer region;

a first plurality of electrical connections on said outer region spaced apart by a first distance; and,

a second plurality of electrical connections on said central region spaced apart by a second distance, wherein said second distance is smaller than said first distance.

24. The apparatus of claim 23 wherein said first and second plurality of electrical connections are selected from the group comprising: input/output connections, power connections, and ground connections.

25. The apparatus of claim 23 further comprising a plurality of routing channels extending from said first and second plurality of electrical connections, wherein said second electrical connections have more routing channels extending therefrom than said first electrical connections.

26. The apparatus of claim 25 wherein said first plurality of electrical connections are spaced apart to allow at least four routing channels to pass between said first plurality of electrical connections, and said second plurality of electrical connections do not have a routing channel between said second plurality of electrical connections.

27. The apparatus of claim 23 wherein said first and second electrical connections are positioned on said surface in a progressive pitch layout.